WHAT IS CLAIMED IS:

1. A routing apparatus for obtaining routing data conforming to a destination address of a packet that arrives from a line, adding the routing data onto the packet, and switching the packet based upon the routing data to send the packet to a prescribed line, comprising:

a main controller having a routing data generator for generating routing data conforming to a requested destination address and sending the routing data to a requesting source;

a line interface for extracting a destination address from a packet that arrives from a line, generating routing-data request for requesting said main controller to be notified of routing data conforming to this destination address, adding the routing data of which notification has been given by said main controller onto the packet and then outputting the packet; and

a switch for sending the routing data request, which enters from a prescribed line interface, to the main controller, sending the routing data from said main controller to a line interface of the requesting source, and switching a packet with attached routing data based upon the routing data to thereby send the packet to another line interface.

2. The apparatus according to claim 1, wherein said routing data generator of said main controller includes:

an associative memory for storing routing data;

a key-data memory for storing key data conforming to destination addresses;

a converter which, when key data conforming to the requested destination address exists in said key-data memory, is for converting this key data to an address of said associative memory; and

a routing-data sending unit for reading routing data out of the associative memory from this address and sending this routing data to the line interface that is the requesting source.

3. The apparatus according to claim 2, wherein said main controller is provided in duplicate to furnish a working main controller and a standby main controller;

when the working main controller updates content stored in each of said memories, said main controller updates also content stored in each of the memories of the standby main controller; and

when the working main controller develops a failure, the standby main controller continues routing control by serving as a new working main controller.

4. The apparatus according to claim 2, wherein said main controller has routing data generators that are associated with respective ones of line speeds;

said line interface adds a line identifier onto a destination address of a packet that arrives from a line so that the routing-data request is created and requests said main controller to be notified of routing data; and

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said main controller responds to the request by generating routing data from whichever routing data generator corresponds to a line speed indicated by the line identifier and sending this routing data to the line interface that is the requesting source.

5. The apparatus according to claim 4, wherein lines having any line speeds are connected to said line interface.

6. The apparatus according to claim 2, wherein each line interface adds a key flag onto a packet for the routing-data request to be sent to said main controller, adds a data flag onto a packet and inputs the result to said switch; and

said switch sends the packet with the attached key flag to said main controller and sends the packet with the attached data flag to a line interface on the output side based upon the routing data.

7. The apparatus according to claim 2, wherein said associative memory and said key-data memory are constituted by contiguous key-data and associative-data storage areas, respectively, of a single memory array;

an entry count e, which is the number of items of key data and the number of items of associative data that can be registered, is calculated in accordance with the following equation:

$$e = y/(k+r)$$

where y represents the total number of single-byte cells of said memory array, the width of the key data is k

bytes and the width of the associative data inclusive of routing data is r bytes; and

read/write control is performed for reading and writing the key data and associative data from and to said key-data storage area and associative-data storage area, respectively, of said memory array based upon k, r and e.

8. The apparatus according to claim 7, wherein said routing data generator further includes:

a register for holding the width k of key data, the width r of associative data and the entry count e; and

an address decoder for performing read/write control of key data and associative data based upon k, r and e.

9. The apparatus according to claim 7, wherein said routing data generator further includes:

holding means which, when multiple items of key data that are identical with key data conforming to the requested destination address or multiple items of key data that are identical with a non-masked portion of the key data conforming to this destination address have been entered in said key-data memory, is for holding the number of entries and the entry key data; and

means for notifying an external processor of the number of entries and entry key data.